UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,334	03/29/2004	Linden Cornett	P18440	5113

46915 7590 07/22/2008

KONRAD RAYNES & VICTOR, LLP.
ATTN: INT77
315 SOUTH BEVERLY DRIVE, SUITE 210
BEVERLY HILLS, CA 90212

EXAMINER	
RUBIN, BLAKE J	

ART UNIT	PAPER NUMBER
2157	

MAIL DATE	DELIVERY MODE
07/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,334	CORNETT, LINDEN	
	Examiner	Art Unit	
	BLAKE RUBIN	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-17,19-21 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17,19-21 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed April 24, 2008.

2. Claims 1, 3-9, 11-17, 19-21, and 23-28 are pending in this application. Claims 1, 3, 4, 6, 8, 9-12, 14, 16, 17, 19-21, 23, 24, and 25-28 are amended. Claims 2, 10, 18, and 22 are cancelled.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-9, 11-17, 19-21, and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaniyar et al (US Publication No. 2003/0187914, hereinafter Kaniyar), in view of Rogers et al (US Patent No. 6,970,990, hereinafter Rogers).

5. With respect to claim 1, Kaniyar discloses a method, comprising:

determining a number of conflicting entries (paragraph [0041], lines 8-18; *where*by *the number of conflicting entries is maintained by a "counter" after determining whether "processor #N exists"*) in a software redirection table having a first set of entries (paragraph [0031], lines 8-12; Figure 3a; *whereby the "data packet*

descriptor....stored in a memory array 345" anticipated the first redirection table), wherein the first set of entries is capable of being mapped (paragraph [0033], lines 3-6) to a second set of entries of a hardware redirection table (paragraph [0034], lines 6-16; Figure 3a; *whereby the "receive queue 355a" anticipated the second redirection table*); and

mapping the first set of entries to the second set of entries, based on the number of conflicting entries in the software redirection table (paragraph [0043], lines 16-28), wherein a conflict is caused if at least two entries of the software redirection table (paragraph [0031], lines 8-12) that are capable of being mapped (paragraph [0008], lines 10-14) to one entry of the hardware redirection table (paragraph [0034], lines 6-16) indicate different receive queues (paragraph [0043], lines 16-28), and indicating that packets associated with conflicting entries are to be directed to one receive queue (paragraph [0043], lines 16-28). Kaniyar does not disclose a threshold.

However, Rogers discloses the method whether the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2; *whereby the number of entries is based on the size of the table*), wherein the number of conflicting entries are determined in response to determining that the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2); determining that the number of conflicting entries is less than a threshold (column 7, lines 53-57).

It would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Kaniyar with the teachings of Rogers. The motivation to do so being, to limit the amount of hardware memory displaced by the table.

6. With respect to claim 3, Kaniyar and Rogers disclose the method of claim 1. Kaniyar further discloses wherein the one receive queue is a first receive queue, the method further comprising:

distributing those packets that are in the first receive queue among all processors of a plurality of processors for processing (paragraph [0043], lines 21-23);

processing those packets that are in a second processing queue in a first processor of the plurality of processors (paragraph [0043], lines 23-28); and

processing those packets that are in a third receive queue in a second processor of the plurality of processors (paragraph [0043], lines 23-28).

7. With respect to claim 4, Kaniyar and Rogers disclose the method of claim 1. Kaniyar further disclose indicating that all packets are to be directed to a single receive queue (paragraph [0043], lines 16-23).

8. And Rogers discloses determining that the number of conflicting entries is not less than the threshold (column 7, lines 53-57).

9. With respect to claim 5, Kaniyar and Rogers disclose the method of claim 4. Kaniyar further discloses processing receive side scaling in software (paragraph [0007],

lines 10-12; paragraph [0008], lines 1-5), wherein processing receive side scaling further comprises creating virtual queues (paragraph [0047], lines 16-18; paragraph [0007], lines 10-12) and queuing deferred procedure calls (paragraph [0004], lines 11-14) to corresponding processors via a device driver (paragraph [0029], lines 19-24).

10. With respect to claim 6, Kaniyar and Rogers disclose the method of claim 1. Rogers further discloses programming the hardware redirection table in accordance with the software redirection table, in response to determining that the first set of entries in the software redirection table does not have more members than the second set of entries in the hardware redirection table (column 11, line 67; column lines 1-2).

11. With respect to claim 7, Kaniyar and Rogers disclose the method of claim 1, wherein determining and mapping are performed by a device driver (paragraph [0029], lines 17-24, paragraph [0033], lines 3-6) in a computational platform having a plurality of processors (paragraph [0026]).

12. With respect to claim 8, Kaniyar and Rogers disclose the method of claim 1, wherein the software redirection table is associated with an operating system (paragraph [0029], lines 12-16) that supports receive side scaling (paragraph [0022]), wherein the hardware redirection table is implemented in a hardware device (paragraph [0034], lines 6-16) coupled to a computational platform having a plurality of processors (paragraph [0026]). Kaniyar does not disclose a fixed size table.

And, Rogers discloses a table is of a fixed size (column 7, lines 15-17).

13. With respect to claim 9, Kaniyar and Rogers disclose a system, comprising:

at least one processor (paragraph [0027], line 2);

a network interface coupled to the at least one processor (paragraph [0027], lines 9-12); and

program logic including code (paragraph [0029], lines 19-24) that is capable of causing the at least one processor to be operable to:

(i) determine a number of conflicting entries (paragraph [0041], lines 8-18) in a software redirection table having a first set of entries (paragraph [0031], lines 8-12), wherein the first set of entries is capable of being mapped (paragraph [0033], lines 3-6) to a second set of entries of a hardware redirection table (paragraph [0034], lines 6-16) implemented in the network interface (paragraph [0047, lines 10-18); and

(ii) map the first set of entries to the second set of entries, based on the number of conflicting entries in the software redirection table (paragraph [0043], lines 16-28), wherein the conflicting entries are caused if at least two entries of the software redirection table (paragraph [0031], lines 8-12) that are capable of being mapped (paragraph [0008], lines 10-14) to one entry of the hardware redirection table (paragraph [0034], lines 6-16) indicate different receive queues (paragraph [0043], lines 16-28), wherein the program logic (paragraph [0029],

lines 19-24) is further capable of causing the at least one processor to be operable to:

(b) indicate that packets associated with conflicting entries are to be directed to one receive queue (paragraph [0043], lines 16-28). But, Kaniyar does not disclose a threshold.

However, Rogers discloses the method

(a) determining whether the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2; *whereby the number of entries is based on the size of the table*), wherein the number of conflicting entries are determined in response to determining that the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2);

(b) determining that the number of conflicting entries is more than a threshold (column 7, lines 53-57).

It would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Kaniyar with the teachings of Rogers. The motivation to do so being, to limit the amount of hardware memory displaced by the table.

14. With respect to claim 11, Kaniyar and Rogers disclose the system of claim 9. Kaniyar further discloses wherein the one receive queue is a first receive queue, wherein the program logic is further capable of causing the at least one processor to be operable to:

distribute those packets that are in the first receive queue among all processors of a plurality of processors for processing (paragraph [0043], lines 21-23);

process those packets that are in a second processing queue in a first processor of the plurality of processors (paragraph [0043], lines 23-28); and

process those packets that are in a third receive queue in a second processor of the plurality of processors (paragraph [0043], lines 23-28).

15. With respect to claim 12, Kaniyar and Rogers disclose the system of claim 9. Kaniyar further discloses wherein the program logic is further capable of causing the at least one processor to be operable to: indicate that all packets are to be directed to a single receive queue (paragraph [0043], lines 16-23)

16. And Rogers disclose the number of conflicting entries is not less than the threshold (column 7, lines 53-57).

17. With respect to claim 13, Kaniyar and Rogers disclose the system of claim 12. Kaniyar further discloses a device driver (paragraph [0029], lines 19-24), wherein the device driver is operable to process receive side scaling in software (paragraph [0007], lines 10-12; paragraph [0008], lines 1-5) by creation of virtual queues (paragraph [0047], lines 16-18; paragraph [0007], lines 10-12), and wherein the device driver is capable of queuing deferred procedure calls (paragraph [0004], lines 11-14) associated with the virtual queues to corresponding processors (paragraph [0009], lines 11-13).

18. With respect to claim 14, Kaniyar and Rogers disclose the system of claim 9. Rogers further discloses the program logic is further capable of causing the at least one processor to be operable to: program the hardware redirection table in accordance with the software redirection table, in response to the determination that the first set of entries in the software redirection table does not have more members than the second set of entries in the hardware redirection table (column 11, line 67; column lines 1-4).

19. With respect to claim 15 Kaniyar and Rogers disclose the system of claim 9, further comprising: a device driver (paragraph [0029], lines 17-24) operable to determine the number of conflicting entries (paragraph [0041], lines 8-18) and map the first set of entries (paragraph [0033], lines 3-6).

20. With respect to claim 16, Kaniyar disclose the system of claim 9, wherein the software redirection table is associated with an operating system (paragraph [0029], lines 12-16) that supports receive side scaling (paragraph [0022]), wherein the hardware redirection table is implemented in the network interface (paragraph [0036], lines 1-6; Figure 3c). Kaniyar does not disclose a fixed size table.

21. However, Rogers discloses a table is of a fixed size (column 7, lines 15-17). It would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Kaniyar with the teachings of Rogers. The motivation to do so being, to limit the amount of hardware memory displaced by the table.

22. With respect to claim 17, Kaniyar and Rogers disclose a system, comprising:

a computational platform (paragraph [0026]);

a storage controller implemented in the computational platform;

at least one processor (paragraph [0027], line 2) coupled to the computational platform;

a network interface (paragraph [0027], lines 9-12) coupled to computational platform; and

program logic including code (paragraph [0029], lines 19-24) that is capable of causing the at least one processor to be operable to:

(i) determine a number of conflicting entries (paragraph [0041], lines 8-18) in a software redirection table having a first set of entries (paragraph [0031], lines 8-12), wherein the first set of entries is capable of being mapped (paragraph [0033], lines 3-6) to a second set of entries of a hardware redirection table (paragraph [0034], lines 6-16), wherein the hardware redirection table is implemented in the network interface (paragraph [0047, lines 10-18); and

(ii) map the first set of entries to the second set of entries, based on the number of conflicting entries in the software redirection table (paragraph [0043], lines 16-28), wherein a conflict is caused if at least two entries of the software redirection table (paragraph [0031], lines 8-12) that are capable of being mapped (paragraph [0008], lines 10-14) to one entry of the hardware redirection table (paragraph [0034], lines 6-16) indicate different receive queues (paragraph [0043], lines 16-28), wherein the program

logic (paragraph [0029], lines 19-24) is further capable of causing the at least one processor to be operable to:

(b) indicate that packets associated with conflicting entries are to be directed to one receive queue (paragraph [0043], lines 16-28). Kaniyar does not disclose a threshold.

However, Rogers discloses the method

(a) determining whether the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2; *whereby the number of entries is based on the size of the table*), wherein the number of conflicting entries are determined in response to determining that the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2);

(b) determining that the number of conflicting entries is less than a threshold (column 7, lines 53-57).

It would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Kaniyar with the teachings of Rogers. The motivation to do so being, to limit the amount of hardware memory displaced by the table.

23. With respect to claim 19, Kaniyar and Rogers disclose the system of claim 17. Kaniyar further discloses wherein the one receive queue is a first receive queue,

wherein the program logic is further capable of causing the at leas one processor to be operable to:

distribute those packets that are in the first receive queue among all processors of a plurality of processors for processing (paragraph [0043], lines 21-23);

process those packets that are in a second processing queue in a first processor of the plurality of processors (paragraph [0043], lines 23-28); and

process those packets that are in a third receive queue in a second processor of the plurality of processors (paragraph [0043], lines 23-28).

24. With respect to claim 20, Kaniyar and Rogers disclose the system of claim 17. Kaniyar further discloses the program logic is further capable of causing the at least one processor to be operable to: indicate that all packets are to be directed to a single receive queue paragraph [0043], lines 16-23).

And Rogers discloses the determination that the number of conflicting entries is not less than the threshold (column 7, lines 53-57).

25. With respect to claim 21, Kaniyar and Rogers disclose an article of manufacture, comprising a storage medium having stored therein instructions that are operable by a machine (paragraph [0028], lines 1-10) to:

determine a number of conflicting entries (paragraph [0041], lines 8-18) in a software redirection table having a first set of entries (paragraph [0031], lines 8-12), wherein the first set of entries is capable of being mapped (paragraph [0033], lines 3-6)

to a second set of entries of a hardware redirection table (paragraph [0034], lines 6-16); and

map the first set of entries to the second set of entries, based on the number of conflicting entries in the software redirection table (paragraph [0043], lines 16-28), and wherein a conflict is caused if at least two entries of the software redirection table (paragraph [0031], lines 8-12) that are capable of being mapped (paragraph [0008], lines 10-14) to one entry of the hardware redirection table (paragraph [0034], lines 6-16) indicate different receive queues (paragraph [0043], lines 16-28), wherein the instructions are further operable by a machine to

(b) determine that packets associated with conflicting entries are to be directed to one receive queue (paragraph [0043], lines 16-28). Kaniyar does not disclose a threshold.

However, Rogers discloses the method

(a) determining whether the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2; *whereby the number of entries is based on the size of the table*), wherein the number of conflicting entries are determined in response to determining that the first set of entries in the table has more members than the second set of entries in the table (column 11, line 67; column 68, lines 1-2);

(b) determining that the number of conflicting entries is less than a threshold (column 7, lines 53-57).

It would have been obvious to one skilled in the art at the time the invention was made to combine the teachings of Kaniyar with the teachings of Rogers. The motivation to do so being, to limit the amount of hardware memory displaced by the table.

26. With respect to claim 23, Kaniyar and Rogers disclose the article of manufacture of claim 21. Kaniyar further discloses whereing the one receive queue is a first receive queue, wherein the instructions are further operable to:

distribute those packets that are in the first receive queue among all processors of a plurality of processors for processing (paragraph [0043], lines 21-23);

process those packets that are in a second processing queue in a first processor of the plurality of processors (paragraph [0043], lines 23-28); and

process those packets that are in a third receive queue in a second processor of the plurality of processors (paragraph [0043], lines 23-28).

27. With respect to claim 24, Kaniyar and Rogers disclose the article of manufacture of claim 21. Kaniyar further discloses the instructions are further operable by a machine to: indicate that all packets are to be directed to a single receive queue paragraph [0043], lines 16-23)

And Rogers discloses determining that the number of conflicting entries is not less than the threshold (column 7, lines 53-57).

28. With respect to claim 25, Kaniyar and Rogers disclose the article of manufacture of claim 24. Kaniyar further disclose the instructions are further operable by a machine to: process receive side scaling (paragraph [0007], lines 10-12; paragraph [0008], lines 1-5) in by creation of virtual queues (paragraph [0047], lines 16-18; paragraph [0007], lines 10-12), wherein a device driver is capable of queuing deferred procedure calls (paragraph [0004], lines 11-14) associated with the virtual queues to corresponding processors (paragraph [0009], lines 11-13).

29. With respect to claim 26, Kaniyar and Rogers disclose the article of manufacture of claim 21. Rogers further discloses the instructions are further operable by a machine to: program the hardware redirection table in accordance with the software redirection table, in response to determining that the first set of entries in the software redirection table does not have more members than the second set of entries in the hardware redirection table (column 11, line 67; column lines 1-4).

30. With respect to claim 27, Kaniyar and Rogers disclose the article of manufacture of claim 21, wherein determination of the number of conflicting entries (paragraph [0041], lines 8-18) and mapping the first set of entries (paragraph [0033], lines 3-6) are performed by a device driver (paragraph [0029], lines 17-24) in a computational platform having a plurality of processors (paragraph [0026]).

31. With respect to claim 28, Kaniyar and Rogers disclose the article of manufacture of claim 21, wherein the software redirection table is associated with an operating system (paragraph [0029], lines 12-16) that supports receive side scaling (paragraph [0022]), wherein the hardware redirection table is implemented in the network interface (paragraph [0036], lines 1-6; Figure 3c). Kaniyar does not disclose a fixed size table.

However, Rogers discloses a table is of a fixed size (column 7, lines 15-17).

Response to Arguments

32. Applicant's arguments filed April 24, 2008 have been fully considered but they are not persuasive. Applicant has amended independent claims 1, 9, 17, and 21 with the requirements of dependent claims 2, 10, 18, and 22.

33. With respect to currently amended claim 1, Applicant argues that the claim requirements differ from Rogers because the claim requires "determining whether the first set of entries in the software redirection table has more members than the second set of entries in the hardware redirection table, wherein the number of conflicting entries are determines in response to determining that the first set of entries in the software redirection table has more members than the second set of entries in the hardware redirection table".

The examiner respectfully disagrees with the applicants arguments. Rogers discloses software redirection tables in the form of "software page from table (SWPFT)" (column 6, line 9), and hardware redirection tables in the form of a "hardware page

frame table (HWPFT)" (column 6, lines 11-12). Rogers further discloses conflicts in the form of "page faults" (column 6, line 22) resulting from a discrepancy in the number of entries between the SWPFT and the HWPFT (column 6, lines 20-33).

34. With respect to currently amended claim 1, Applicant further argues that the claim requirements differ from Rogers because the claim recites "fault" while Rogers recites "page faults". The applicant goes on to explain that conflicting entries of the claim requirements are caused if at least two entries of the software redirection table that are capable of being mapped to one entry of the hardware redirection table indicate different receive queues.

The examiner respectfully disagrees with the applicants arguments. Rogers discloses "page faults" which are embodied within Rogers to teach the applicant's claimed "faults". Rogers discloses a "virtual segment identifier (VSID)" (column 10, line 67) and "abbreviated page index (API)" (column 10, line 67; column 11, line 1) which together make up a virtual address, which is the equivalent of an entry in the software redirection table. These addresses are complemented by their hardware redirection table entry counterparts in Rogers when they are pinned page table entries (column 11, lines 3). The conflict occurs when these two entries diverge away from pointing to the same location as anticipated by the nature of their pairing (column 11, lines 30-34).

Conclusion

35. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BLAKE RUBIN whose telephone number is (571) 270-3802. The examiner can normally be reached on M-R: 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BJR

/Ario Etienne/
Supervisory Patent Examiner, Art Unit 2157